Counsel listed on signature page

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

CASE NO. 3:17-cv-05671-BLF

JOINT CASE MANAGEMENT STATEMENT & [PROPOSED] ORDER

Judge: Hon. Beth Labson Freeman
Date: December 21, 2017
Time: 11:00 a.m.
Location: Courtroom 3, 5th Floor

Date Complaint Filed: October 2, 2017

Trial Date: None Set

Pursuant to Federal Rule of Civil Procedure 26(f), Civil Local Rule 16-9, Patent Local Rule 2-1(b), the Standing Order for All Judges of the Northern District of California – Contents of Joint Case Management Statement, Judge Freeman's Standing Order re Civil Cases and the October 13, 2017 Notice Resetting Case Management Conference Following Reassignment (Dkt. No. 15), Plaintiff VLSI Technology, LLC ("VLSI") and Defendant Intel Corporation ("Intel") jointly submit this Case Management Statement and Proposed Order.

A. JURISDICTION AND SERVICE

This is an action for alleged patent infringement arising under the patent laws of the United States, 35 U.S.C. § 101 et seq. The Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). Defendant Intel has been served. No other parties remain to be served. No issues exist regarding personal jurisdiction, venue, or service.

B. BRIEF DESCRIPTION OF THE CASE AND DEFENSES, AND EVENTS UNDERLYING THE ACTION

VLSI filed its Complaint on October 2, 2017. (Dkt. No. 1.) VLSI alleges that Intel infringes United States Patent Nos. 7,268,588 ("'588 patent"); 7,675,806 ("'806 patent"); 7,706,207 ("'207 patent"); 7,709,303 ("'303 patent"); 8,004,922 ("'922 patent"); 8,020,014 ("'014 patent"); and 8,268,672 ("'672 patent"); 8,566,836 ("'836 patent") (collectively, the "Patents-in-Suit") by making, using, offering for sale, selling, and/or importing microprocessors and Field Programmable Gate Arrays in violation of 35 U.S.C. § 271. VLSI seeks an award of damages pursuant to 35 U.S.C. § 284.

On December 6, 2017, Intel filed its Answer, Defenses, and Counterclaims to the Complaint, denying infringement and asserting counterclaims for patent invalidity and non-infringement. (Dkt. No. 39.)

C. THE PRINCIPAL LEGAL AND FACTUAL ISSUES IN DISPUTE

The legal and factual issues set forth below are not intended to be final or exhaustive, and the parties reserve the right to reformulate these issues, raise additional issues, dispute that there

are issues, or include any other appropriate issues as they develop or become known to the parties through the course of discovery and investigation. Further, the characterization of an issue as "factual" or "legal" is not a concession that it is not the other or both.

The principal disputed factual issues are:

1. Whether any Intel products infringe any of the Patents-in-Suit pursuant to 35 U.S.C. § 271.
2. For any Patent-in-Suit found to be both valid and infringed, the amount of damages.
3. Whether the Patents-in-Suit are invalid and/or unenforceable.
4. Whether this case is exceptional under 35 U.S.C. § 285, and, if so, whether either party is entitled to an award of attorney fees.

The principal disputed legal issues are:

1. The proper construction of any disputed patent claim terms.
2. Whether Intel infringes any of the asserted claims of the Patents-in-Suit pursuant to 35 U.S.C. § 271.
3. Whether any of the asserted claims of the Patents-in-Suit is invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.
4. Whether any of the asserted claims of the Patents-in-Suit is unenforceable.
5. The amount of damages, if any, due to VLSI pursuant to 35 U.S.C. § 284.
6. Whether VLSI is entitled to enhanced damages pursuant to 35 U.S.C. § 284.
7. Whether VLSI's claims are barred, precluded, or otherwise improper based on one or more of Intel's affirmative defenses.
8. Whether VLSI's claims for damages are barred or limited based on 35 U.S.C. §§ 286 and/or 287.

D. MOTIONS AND/OR PENDING MATTERS

No motions are outstanding in this matter.

The parties anticipate claim construction briefing under the Patent Local Rules and expect that they may file motions for summary judgment of infringement/non-infringement and/or patent

validity/invalidity.

E. AMENDMENT OF PLEADINGS

Discovery will dictate whether any additional parties, claims, or counterclaims are needed. The parties propose the deadline in Section Q (Scheduling), Exhibit A, as the deadline for amending the pleadings without leave of the Court.

F. EVIDENCE PRESERVATION

The parties certify that they have reviewed the Guidelines Relating to the Discovery of Electronically Stored Information ("ESI Guidelines"), and confirm that the parties have met and conferred pursuant to Fed. R. Civ. P. 26(f) regarding reasonable and proportionate steps taken to preserve evidence relevant to the issues reasonably evident in this action. The parties anticipate that they will submit an ESI Stipulation setting forth their agreements with respect to the discovery of ESI in this action.

G. INITIAL DISCLOSURES

The parties will exchange Initial Disclosures pursuant to Fed. R. Civ. P. 26(a)(1) on December 14, 2017.

H. DISCOVERY

Discovery taken to date:

On Wednesday, November 29, 2017, after the parties conducted their Rule 26(f) conference, VLSI and Intel both served a First Set of Interrogatories and a First Set of Requests for Production.

Scope of anticipated discovery:

VLSI intends to pursue discovery relating to the claims for patent infringement, Intel's defenses and counterclaims thereto, damages, and prayers for relief.

Intel intends to pursue discovery relating to the factual and legal issues set forth herein above and in its Answer, Defenses, and Counterclaims. Intel anticipates that this discovery will include at least the following: (1) the conception, reduction to practice, and any alleged diligence in reduction to practice of the inventions claimed by the Patents-in-Suit; (2) prior art to the Patents-in-Suit; (3) the validity of the Patents-in-Suit; (4) the prosecution of the Patents-in-Suit,

including the applicants' disclosure of prior art to the Patent Office; (5) title and ownership of the Patents-in-Suit; (6) licensing of the Patents-in-Suit; (7) any damages claimed by VLSI; (8) VLSI's basis for its claims of infringement; and (9) the construction of any disputed claim terms of the Patents-in-Suit.

Limits on Discovery:

1. **Requests for Production of Documents and Things**

The parties agree to no limits on requests for production of documents and things.

2. **Interrogatories**

Each party shall be permitted to serve a maximum of 50 interrogatories on any other party.

3. **Request for Admissions**

VLSI's Proposal: Each party may serve up to 50 requests for admission. However, there is no limit on the number of requests for admission the parties may serve to establish the admissibility of documents. Requests for admission directed to document admissibility shall be clearly denoted as such and shall be served separately from any request for admission subject to the numerical limitations stated above.

Intel's Proposal: Each party may serve up to 150 requests for admission. However, there is no limit on the number of requests for admission the parties may serve to establish the admissibility of documents. Requests for admission directed to document admissibility shall be clearly denoted as such and shall be served separately from any request for admission subject to the numerical limitations stated above.

4. **Fact Depositions**

VLSI's Proposal: Each party shall have 100 hours of total deposition time per side (not including expert depositions), to take the depositions of party and non-party witnesses, as the party sees fit. For corporate depositions under Fed. R. Civ. P. 30(b)(6), the time limits of the deposition shall not be governed by the 7-hour limit of Fed. R. Civ. P. 30(d)(1) but shall be subject only to the total time limits set out above. If a corporate deposition lasts longer than 7 hours, it will extend to another day. For individual witnesses designated by a party for multiple topics contained in a 30(b)(6) notice, the parties will work in good faith to agree to a reasonable number

of hours per designated witness depending on the number of topics for which each witness is designated. The parties agree that individual depositions that require the use of a translator shall be limited to 14 hours, only 7 hours of which will count against that party's total deposition time. The parties agree to meet in good faith should either party request additional time to take depositions.

Intel's Proposal: Each party shall have 100 hours of total fact deposition time per party (not counting expert depositions) to take the depositions of each party's witnesses, including corporate depositions under Fed. R. Civ. P. 30(b)(6) depositions. In addition, each party shall have 100 hours of total fact deposition time to take the deposition of third parties. Each deposition shall be governed by the one-day, seven-hour limit of Fed. R. Civ. P. 30(d)(1), with each deposition counting at least 3.5 hours. The deposition of any single individual designated as a corporate witness to testify regarding a deposition topic contained in a deposition notice served under Fed. R. Civ. P. 30(b)(6) is presumptively limited to seven (7) hours of deposition testimony for that individual, with each deposition counting at least 3.5 hours. However, if an individual Fed. R. Civ. P. 30(b)(6) corporate witness is designated by the offering party on multiple unrelated topics, the deposing party may request a reasonable number of additional deposition hours, and the offering party shall not unreasonably deny the request. Depositions that require the use of a translator shall be limited to 14 hours (including depositions of third parties), and only half the total time used in the deposition will count towards the deposition time limit.

5. **Expert Depositions**

The parties agree that each party may depose each expert for a total of seven (7) hours per patent on which that expert opines on issues of infringement/noninfringement and/or validity/invalidity. For example, if an expert submits reports on (in)validity and on (non)infringement regarding two patents, that expert may be deposed for a total of up to fourteen (14) hours; specifically, up to seven (7) hours per patent. For experts who offer opinions on more than one patent, the party taking the deposition shall provide one week's notice of the day on which the expert will be questioned on each patent. Questions about a specific patent will be limited to the day on which the party taking the deposition has given notice. Questions about

other patents will not be allowed on that day, except to the extent that the questions relate to issues on which the examiner believes in good faith the expert may be taking inconsistent positions. An expert who offers opinions on more than one patent may be questioned by a different lawyer for each patent. Each party may also take a total of seven (7) hours of expert deposition testimony of each other expert.

6. **Protective Order**

The parties will be producing confidential information requiring entry of a protective order in this action. Any confidential information produced before entry of a Protective Order is subject to the Northern District of California model protective order for litigation involving patents (pursuant to Patent L.R. 2-2). The parties intend to meet and confer in good faith to reach agreement on the terms of a stipulated Protective Order, and will advise the Court if they are unable to resolve any disputed issues. The parties intend to file the stipulated Protective Order (with competing provisions if necessary) by the date shown in section Q (Scheduling), Exhibit A.

7. **Electronic Discovery**

The parties will be collecting and producing relevant Electronically Stored Information ("ESI"). The parties hereby certify that they have reviewed the Court's Guidelines for the Discovery of Electronically Stored Information and discussed the issues listed in the Court's Checklist for Rule 26(f) Meet and Confer Regarding Electronically Stored Information. The parties intend to meet and confer in good faith to reach agreement on the terms of a stipulated ESI Order, and will advise the Court if they are unable to resolve any disputed issues. The parties intend to file the stipulated ESI Order (with competing provisions if necessary) by the date shown in section Q (Scheduling), Exhibit A.

8. **Discovery from Experts**

The parties agree that except for the deposition time limits set forth above, discovery of experts is governed by Fed. R. Civ. P. 26(b)(4), except that each party shall bear the cost of its own experts, notwithstanding Rule 26(b)(4)(E). The parties further agree that communications between experts and counsel and any resulting work product, including, but not limited to, draft reports and notes, will not be discoverable, with the exception of an expert's billing records, which

will be produced if requested by the opposing party. Detailed descriptions of work contained in the expert's billing records may be redacted to avoid disclosure of the expert's work product or substantive communications with counsel.

9. **Service**

The parties agree that, to the extent possible in light of the volume of the submission, all court filings, discovery, and documents to be served on opposing counsel, to the extent not served through ECF (namely, filings under seal), will be served via email, or if too voluminous, by FTP or other internet file service, on each of the other parties, and such service shall constitute proper service under Fed. R. Civ. P. 5(b)(2)(E). The additional three-day period for service under Fed. R. Civ. P. 6(d) does not apply.

10. **Privilege Logs/Privileged Information**

VLSI's Proposal: Except as necessary to comply with Patent L.R. 3-7 (Advice of Counsel), the parties are not required to include on their privilege logs any protected documents that came into existence on or after the date of filing the complaint. Except as necessary to comply with Patent L.R. 3-7, the parties are not required to include on their privilege logs any protected documents that reflect communications between counsel and their respective clients, or work product documents that reflect work of counsel that were created in anticipation of this litigation, even if created before the filing date of the complaint.

Intel's Proposal: Except as necessary to comply with Patent L.R. 3-7 (Advice of Counsel), the parties are not required to include on their privilege logs any protected documents that came into existence on or after the date of filing the complaint.

I. CLASS ACTIONS

Not applicable.

J. RELATED PENDING CASES

There are currently no related pending cases.

K. RELIEF

VLSI seeks a judgment that Intel has infringed and continues to infringe the Patents-in-Suit under 35 U.S.C. § 271. VLSI further seeks damages adequate to compensate for the infringement

by Intel, including enhanced damages and attorneys' fees, together with interest and costs under 35 U.S.C. §§ 284 & 285. VLSI additionally seeks a compulsory ongoing royalty.

Intel seeks (1) a declaratory judgment that it has not infringed the Patents-in-Suit, directly or indirectly, and that the Patents-in-Suit are invalid, (2) an order dismissing the Complaint with prejudice, and (3) an award of its attorney fees and costs pursuant to 35 U.S.C. § 285.

L. SETTLEMENT AND ADR

The parties have met-and-conferred pursuant to ADR L.R. 3-5 and have stipulated to private mediation within 30 days of the Court's Markman Order. (Dkt. No. 38.)

M. CONSENT TO MAGISTRATE JUDGE

The parties decline to proceed before a magistrate judge.

N. OTHER REFERENCES

The parties do not believe that this case is suitable for reference to binding arbitration, a special master, or the Judicial Panel on Multidistrict Litigation.

O. NARROWING OF ISSUES

VLSI's Proposal: VLSI agrees that its infringement contentions and Intel's invalidity contentions will need to be progressively narrowed throughout the pre-trial proceedings to simplify the case for the jury. VLSI believes this should be done in a two-phase approach, rather than Intel's three-phase approach, by eliminating Intel's proposed first phase. VLSI's two-stage proposal is the approach taken by this Court in previous patent cases. *See, e.g, Finjan v. Cisco*, 5:17-cv-00072-BLF, Dkt. 70, at 4 (two-phase narrowing without an equivalent to Intel's first phase).

Intel proposes a first phase in which VLSI limits the number of asserted claims in its L.R. 3-1 infringement contentions. VLSI does not believe that it is appropriate to require that it reduce the number of asserted claims at this early stage, even before Intel is required to disclose its prior art to VLSI. Intel does not cite to any order of this Court requiring a patent owner to limit the number of asserted claims in its L.R. 3-1 infringement contentions, or at any time before the patent owner receives the defendant's L.R. 3-3 invalidity contentions.

VLSI agrees to limit the number of claim terms one week after patent L.R. 4-1 Exchange

of Claim Terms (Intel's Phase 2). VLSI will limit the asserted claims to no more than 10 claims per patent and no more than 56 claims total.

Thirty days after VLSI narrows its asserted claims, VLSI proposes that Intel narrow its prior art to no more than 10 combinations[1] per patent and no more than 40 combinations total.

VLSI agrees to limit the number of asserted claim terms within 30 days of the Court's issuance of its *Markman* ruling to no more than 6 claims per patent and no more than 32 claims total (Intel's Phase 3.)

Thirty days after VLSI's final narrowing, VLSI proposes that Intel limit its prior art to no more than 6 combinations per patent and no more than 20 combinations total.

These proposed limits are consistent with the Court's limits imposed in the *Finjan v. Cisco* case. *See id*., at 4 (for a five-patent case, two stages of narrowing and similar claim/validity theory limitations—for the first stage, patent owner to limit asserted claims to 10 claims per patent and 32 claims total; defendant to limit references to 12 per patent and a total of 40; for the second and final stage, patent owner to limit asserted claims to 5 claims per patent and 16 claims total; defendant to limit references to 6 per patent and a total of 20).

To narrow discovery issues in this case, VLSI further proposes that the parties identify representative Intel accused products. VLSI proposes that this identification be provided to the Court no later than 30 days after Intel provides its discovery under Patent L.R. 3-4.

Intel's Proposal: VLSI has asserted eight patents with a combined 150 claims against Intel, accusing essentially every processor Intel manufactures and sells or has manufactured and sold in the past six years, in addition to other products and technology solutions. Given the massive number of claims in this action, VLSI's overbroad and nonspecific allegations in the Complaint (*i.e.*, accusing "Intel Core i3, i5, and i7 microprocessors; Xeon E3, E5, and E7 microprocessors; Atom microprocessors ***and other Intel microprocessors that incorporate the infringing features*** described below"), and Intel's obligations under Patent L.R. 3-3 (service of

[1] The term "combination" needs to be defined to avoid future disputes. VLSI proposes that "combination" be used in the same way the Court used the term "theory" in its Case Schedule and Order in *Finjan v. Bluecoat*, Case No. 15-cv-03295-BLF, Dkt. 41, at 4 n.3 ("A single anticipation theory is a single reference being asserted for a specific patent. A single obviousness theory is a specific combination of references for a specific patent. A specific combination of references for a single obviousness theory shall not be changed or revised for subsequent election of asserted prior art. . . .")

invalidity contentions for each asserted claim) and Patent L.R. 3-4 (*i.e.*, production of "source code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality" and "documents sufficient to show the sales, revenue, cost, and profits for accused instrumentalities"), the burden of litigation will fall disproportionately on Intel unless the parties agree to limit the scope of the case in a structured manner.

VLSI's main argument for why it should not be required to narrow its claims in its infringement contentions appears to be that it wants the benefit of seeing Intel's prior art first. However, 80 claims—which is (i) more than half the number of claims in the patents-in-suit, (ii) approximately the same number of claims as the Court stated was too many pre-invalidity contentions in *HP v. ServiceNow*, and (iii) approximately the number to which the plaintiff agreed to narrow in *Delphix v. Actifio* pre-invalidity contentions—would still leave VLSI with a very ample number from which to choose after reviewing Intel's invalidity contentions. VLSI's proposal forces Intel to address a large number of patent claims in its invalidity contentions only to have them dropped a short time later by VLSI.

Contrary to VLSI's statements, its proposal is inconsistent with the limits set by the Court in the *Finjan v. Cisco* case. In *Cisco*, the Court limited the patent owner to 32 claims total at the first stage—24 claims fewer than VLSI proposes—and 16 claims total at the second stage—16 claims fewer than VLSI proposes. Yet, VLSI proposes that Intel should be limited to the same number of prior art references as the Court imposed in *Cisco*. As a result, VLSI is proposing that Intel should be limited to ***16 fewer*** combinations than VLSI has asserted patents in its first phase and ***12 fewer*** combinations than VLSI has asserted patents in its second phase. VLSI's proposal should be rejected not only as inconsistent with the Court's past rulings, which allow for more combinations than asserted patent claims, but because it would unduly limit Intel's ability to mount an invalidity defense for the still-large number of claims on which VLSI would be proceeding.

Therefore, consistent with the Court's prior rulings to narrow large patent litigations, Intel proposes three phases of narrowing:

- Phase 1
  - VLSI's L.R. 3-1 Infringement Contentions is limited to 80 claims and no more than 10 claims per patent. *See, e.g.*, *HP v. Service Now*, Case No. 5:14-cv-750-BLF, Dkt. No. 58 at 6 (expressing concern that HP's amended infringement contentions will still contain 84 claims in 8 patent case); *id.* at Dkt. 54 (ordering the parties to propose limits on asserted claims and prior art references); *id.*, Dkt. No. 61 (parties stipulating to no more than 45 claims in amended infringement contentions and no more than 3 grounds for invalidity per asserted patent claim in invalidity contentions); *Delphix v. Actifio*, 5:13-cv-4613, Dkt. No. 67 at 7 (expressing concern about the number of asserted claims where plaintiff had asserted 174); *id.*, Dkt. No. 87 at 22-23 (parties reduced asserted claims by 50% prior to service of invalidity contentions, i.e. plaintiff reduced to no more than 87 claims).
- Phase 2
  - One week after Patent L.R. 4-1 Exchange of Claim Terms, VLSI narrows its asserted claims to no more than 10 per patent and no more than 32 total. *See, e.g.*, *Finjan v. Blue Coat*, Case No. 5:15-cv-03295, Dkt. No. 41 at 5 (in a seven patent case, plaintiff was ordered to make an initial election of 10 claims per patent and no more than 32 total after Patent L.R. 4-1 exchange); *Finjan v. Cisco*, 5:17-cv-00072-BLF, Dkt. 70 at 4 (in a five patent case, plaintiff was ordered to make an initial election of 10 claims per patent and no more than 32 total after Patent L.R. 4-1 exchange); *Finjan v. Proofpoint*, Case No. 4:13-cv-05808, Dkt. No. 98 at 2 (in an eight patent case, plaintiff was ordered to make an initial election of an average of five claims per patent and no more than 40 claims total after Patent L.R. 4-1 exchange).
  - One month after VLSI narrows its asserted claims, Intel narrows its prior art combinations to no more than 14 combinations per patent and no more

than 50 total.[2] *See, e.g.*, *Blue Coat*, Case No. 5:15-cv-03295, Dkt. No. 41 at 5 (in a seven patent case, defendant ordered initially to narrow invalidity defense to no more than 14 obviousness combinations per patent and no more than 46 total); *Cisco*, 5:17-cv-00072-BLF, Dkt. 70 at 4 (in a five patent case, defendant ordered initially to narrow invalidity defense to no more than 12 obviousness combinations per patent and no more than 40 total); *Proofpoint*, Case No. 4:13-cv-05808, Dkt. No. 98 at 2 (in eight patent case, defendant was ordered to initially narrow prior art to six anticipatory references and four obviousness combination per patent).

- Phase 3
  - One month after *Markman* decision, VLSI makes its final narrowing of asserted claims to no more than five per patent and no more than 16 total. *See, e.g.*, *Blue Coat*, Case No. 5:15-cv-03295, Dkt. No. 41 at 5 (plaintiff ordered to make final narrowing of asserted claims to no more than five per patent and no more than 16 total after claim construction order); *Cisco*, 5:17-cv-00072-BLF, Dkt. 70 at 4 (plaintiff ordered to make final narrowing of asserted claims to no more than five per patent and no more than 16 total after claim construction order); *Proofpoint*, Case No. 4:13-cv-05808, Dkt. No. 98 at 2 (plaintiff ordered to make final narrowing of asserted claims to no more than an average of three per patent and 24 total before opening expert reports).
  - One month after VLSI's final narrowing, Intel makes final narrowing of its prior art combinations to no more than 6 per patent and no more than 25 total. *See, e.g.*, *Blue Coat*, Case No. 5:15-cv-03295, Dkt. No. 41 at 5 (defendant ordered to make final selection of invalidity theories to no more than six per patent and 20 total); *Cisco*, 5:17-cv-00072-BLF, Dkt. 70 at 4 (defendant ordered to make final selection of invalidity theories to no more

[2] Invalidity defenses not based on prior art under 35 U.S.C. §§ 102 and 103 (e.g., 35 U.S.C. §§ 101 and 112) will not count as a combination. Each unique combination of one or more references counts as one combination.

than six per patent and 20 total); *Proofpoint*, Case No. 4:13-cv-05808, Dkt. No. 98 at 2 (defendant ordered to make final narrowing of prior art to no more than four anticipatory references and obviousness combinations per patent).

Intel believes it is premature to discuss representative products at this time given that it does not yet even know which products will be accused. Moreover, it is VLSI's burden to identify which products it claims to be representative and why they are in fact representative. Intel therefore does not think it is appropriate to set a deadline by which the parties must agree to representative products.

P. EXPEDITED TRIAL PROCEDURE

The parties do not believe that this case is suitable for the Expedited Trial Procedure of General Order No. 64 Attachment A.

Q. SCHEDULING

The parties specifically reserve their right to request that the schedule be amended due to changes occurring in the course of the case, such as amendments to the pleadings, additions of parties, professional or case conflicts, or other good cause, in accordance with Fed. R. Civ. P. 16(b). Attached as Exhibit A is a table that provides the parties' respective proposed positions on scheduling.

VLSI's Statement: VLSI's schedule up to the *Markman* hearing simply follows the local patent rules. After the *Markman* hearing, VLSI's schedule provides more than adequate time for fact and expert discovery, dispositive motions, and pre-trial disclosures. This leads to a trial in late July and early August 2019, a little less than two years after the October 2, 2017, filing of this action.

Intel's Statement: Consistent with the Court's schedule in its other large patent cases, Intel has proposed a trial date of March 1, 2021, with interim deadlines set accordingly. *See, e.g.*, *Finjan, Inc. v. Cisco Sys., Inc.* (Case No. 5:17-cv-00072) (in a five-patent case filed on January 16, 2017, the Court set trial three years and five months out on June 1, 2020); *Power Integrations, Inc. v. ON Semiconductor Corp., et al*. (Case No. 5:16-cv-06371) (in a fifteen-patent case filed on November 1, 2016, the Court set trial three years and one month out on December 2, 2019); *Space Data Corp. v. Alphabet Inc. and Google LLC* (Case No. 5:16-cv-03260) (in a five-patent case filed on June 13, 2016,

the Court set trial three years out on June 3, 2019). Intel's proposed schedule accounts for the large number of asserted patents and claims, breadth of the accused products, and the complexity of the accused technologies. Intel also anticipates that a large number of third-party prior art related depositions will be required.

R. TRIAL

The parties request that the case be tried to a jury. The parties estimate that the case can be completed in approximately ten court days.

S. DISCLOSURE OF NON-PARTY INTERESTED ENTITIES OR PERSONS.

The parties have filed Certifications of Interested Entities or Persons pursuant to Civil Local Rule 3-16. (Dkt. No. 4 (VLSI's certification); Dkt. No. 40 (Intel's certification).)

VLSI Technology LLC is a subsidiary of CF VLSI Holding LLC, a privately held company. No publicly held corporation owns 10% or more of the plaintiffs' stock.

Pursuant to Civil Local Rule 3-15, VLSI certifies that the following listed persons, associations of persons, firms, partnerships, corporations (including parent corporations), or other entities other than the parties themselves (i) have a financial interest of any kind in the subject matter in controversy or in a party to the proceeding; or (ii) have other kind of interest that could be substantially affected by the outcome of this proceeding:

- CF VLSI Holdings LLC
- Michael Stolarski
- NXP B.V.

Intel certifies that it does not have a parent corporation and no publicly-held corporation owns 10% or more of its stock.

T. PROFESSIONAL CONDUCT

The attorneys of record confirm that they have reviewed the Guidelines for Professional Conduct for the Northern District of California.

U. OTHER MATTERS

Pursuant to Patent Local Rule 2-1(b), the parties have also met and conferred regarding the following additional matters:

1. **Modification of Obligations/Deadlines in Patent Local Rules**

To the extent the parties have proposed any modifications of the obligations or deadlines in the Patent Local Rules, these issues have been raised above.

2. **Claim Construction Discovery and Damages Discovery**

The parties believe it is premature at this time to discuss the scope and timing of claim construction discovery. Each party reserves the right to take the deposition of the other party's expert if the other party relies upon a declaration from its expert during claim construction briefing or to support its damages position.

3. **Format of Claim Construction Hearing**

VLSI believes the *Markman* hearing should be done term-by-term, with plaintiff going first, rebuttal by defendant, and then reply by plaintiff. VLSI does not see a need for live testimony. VLSI asks for a one-day hearing.

Intel believes that the parties should alternate which goes first for each term, and that the parties should proceed with argument in a "ping-pong" fashion thereafter.

4. **How the Parties Intend To Educate the Court on the Technology**

VLSI's Proposal: The parties will prepare separate, non-argumentative audiovisual tutorial presentations regarding the relevant technology to be given to the Court on the date proposed in section Q (Scheduling) before the *Markman* hearing. If it would be helpful to the Court, the parties can provide additional tutorial information or answer the Court's questions on the parties' tutorial presentations at the beginning of the *Markman* hearing.

Intel's Proposal: The parties will prepare separate, non-argumentative audiovisual tutorial presentations regarding the relevant technology to be given to the Court on the date proposed in section Q (Schedule) before the *Markman* hearing. The parties will have a separate Technology Tutorial where each side will have two hours to educate the Court on the underlying technology, ahead of the *Markman* hearing.

5. **Non-binding, good-faith estimate of damages**

VLSI's Position: In accordance with Patent Local Rule 2-1(b)(5), VLSI provides the following non-binding, good-faith estimate of the damages. Based on publicly available information,

VLSI estimates that exposed US sales of accused Intel products ranges from approximately $200 billion to approximately $300 billion. Applying a reasonable royalty analysis, VLSI estimates that the damages will range between $2.6 billion to $5.4 billion. This non-binding good faith estimate of damages is preliminary only. The determination of the appropriate measure of and methodology for computing damages in this case will depend on and be subject to change based on fact and expert discovery in this case.

Intel's Position: Intel does not believe that VLSI is entitled to any damages because Intel has not infringed any valid patent.

Dated: December 14, 2017

By: */s/ Henry C. Bunsow*
Henry C. Bunsow

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Respectfully Submitted,

By: */s/ Mark D. Selwyn*
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Exhibit A – Proposed Case Schedule

DEADLINE	VLSI'S PROPOSED DATES	INTEL'S PROPOSED DATES
Last date to: • Meet and confer re: initial disclosures, early settlement, ADR process selection, and discovery plan • File ADR Certification signed by parties and counsel • File either Stipulation to ADR Process or Notice of Need for ADR Phone Conference	Thursday, November 30, 2017	Thursday, November 30, 2017
Service of Initial Disclosures	Thursday, December 14, 2017	Thursday, December 14, 2017
Initial Case Management Conference	Thursday, December 21, 2017	Thursday, December 21, 2017
Disclosure of asserted claims and infringement contentions & accompanying document production under Patent L.R. 3-1, 3-2 (14 days after Initial Case Management Conference)	Thursday, January 4, 2018	Thursday, January 18, 2018
Proposed ESI Order and Proposed Protective Order	Friday, January 19, 2018	Friday, December 22, 2018
Deadline to serve invalidity contentions and accompanying document production under Patent L.R. 3-3, 3-4 (45 days after Patent L.R. 3-1, 3-2)	Monday, February 19, 2018	Monday, March 19, 2018
Parties to exchange proposed claim terms for construction under Patent L.R. 4-1 (14 days after Patent L.R. 3-3, 3-4)	Monday, March 5, 2018	Monday, April 16, 2018
VLSI's Initial Narrowing of Asserted Claims	Monday, March 12, 2018	Monday, April 23, 2018
Parties to agree to representative products	Wednesday, March 21, 2017	VLSI has the burden of proposing representative products and proving that they are representative. A deadline for agreement is therefore inappropriate.

DEADLINE	VLSI'S PROPOSED DATES	INTEL'S PROPOSED DATES
Parties to exchange preliminary claim constructions and extrinsic evidence under Patent L.R. 4-2 (21 days after Patent L.R. 4-1)	Monday, March 26, 2018	Monday, May 21, 2018
Plaintiff to serve damages contentions under Patent L.R. 3-8 (50 days after Patent L.R. 3-3)	Tuesday, April 10, 2018	Tuesday, May 22, 2018
Intel's Initial Election of Prior Art Combinations	Wednesday, April 11, 2018	Wednesday, May 23, 2018
Parties to file joint Claim Construction Chart and Prehearing Statement including citations to evidence (intrinsic and/or extrinsic) under Patent L.R. 4-3 (Per Pat. L.R. 4-3, not later than 60 days after service of invalidity contentions)	Friday, April 20, 2018	Friday, June 1, 2018
Defendant to serve responsive damages contentions under Patent L.R. 3-9 (30 days after Patent L.R. 3-8)	Thursday, May 10, 2018	Thursday, July 5, 2018
Deadline to complete discovery related to claim construction under Patent L.R. 4-4 (30 days after Patent L.R. 4-3)	Monday, May 21, 2018	Monday, July 15, 2018
VLSI to file opening claim construction briefs under Patent L.R. 4-5(a) (45 days after Patent L.R. 4-3)	Monday, June 4, 2018	Monday, July 30, 2018
Intel to file responsive brief and supporting evidence under Patent L.R. 4-5(b) (14 days after Patent L.R. 4-5(a))	Monday, June 18, 2018	Monday, August 27, 2018
VLSI to file reply brief and any evidence directly rebutting the supporting evidence contained in Intel's response under Patent L.R. 4-5(c) (7 days after Patent L.R. 4-5(b))	Monday, June 25, 2018	Monday, September 27, 2018
Submission of *Markman* tutorial	Tuesday, July 3, 2018	Thursday, December 13, 2018
Technology Tutorial		Thursday, January 17, 2019 (subject to the Court's availability)
Markman Hearing At the Court's convenience (at least 14 days after completion of claim construction briefing)	Thursday, July 12, 2018 (subject to the convenience of the Court's calendar)	Thursday, January 31, 2019 (subject to the Court's availability)
Deadline to Complete Private Mediation ADR	30 days after Markman Order	30 days after Markman Order

DEADLINE	VLSI'S PROPOSED DATES	INTEL'S PROPOSED DATES
Deadline for substantial completion of production of non-email documents and things		Friday, May 17, 2019
Last day to exchange privilege logs	Friday, July 27, 2018	Thursday, August 22, 2019
Amendments to pleadings	Friday, August 16, 2018	Friday, July 20, 2018
VLSI's Final Narrowing of Asserted Claims	30 days after service of Court's Claim Construction Ruling	One month after service of Court's Claim Construction Ruling
Deadline to Disclose any Reliance on Advice of Counsel and Production of Opinion under Patent L.R. 3-7 (30 days after Claim Construction Ruling)	30 days after service of Court's Claim Construction Ruling	30 days after service of Court's Claim Construction Ruling
Intel's Final Election of Prior Art Combinations	30 days after VLSI's Final Narrowing of Asserted Claims	One month after VLSI's Final Narrowing of Asserted Claims
Deadline to Complete Fact Discovery ("close of fact discovery")	Friday, October 19, 2018	Thursday, November 21, 2019
Deadline for Opening Expert Reports by the Party with the Burden of Proof	Tuesday, November 20, 2018	Thursday, February 7, 2020
Deadline for Rebuttal Expert Reports	Friday, December 21, 2018	Thursday, March 19, 2020
Deadline for Reply Expert Reports	Friday, January 18, 2019	Thursday, March 26, 2020
Deadline to Complete Expert Discovery	Friday, February 15, 2019	Thursday, May 7, 2020
Deadline to File Dispositive Motions (Civ. L.R. 7-2(a), at least 35 days before hearing)	Thursday, March 14, 2019 (including Motions for Summary Judgment, Motions to Strike Expert Testimony, or Daubert Motions)	Thursday, June 18, 2020 (only Motions for Summary Judgment)
Deadline to File Responsive Dispositive Motion Briefs		Thursday, July 9, 2020
Deadline to File Reply Dispositive Motion Briefs		Thursday, July 23, 2020
Hearings on summary judgment motions (Judge Freeman's Standing Order for Civil Cases Section F, ". . . at least 90 days before trial")	Thursday, April 18, 2019 (including Motions for Summary Judgment, Motions to	Thursday, August 6, 2020 (only Motions for Summary Judgment)

DEADLINE	VLSI'S PROPOSED DATES	INTEL'S PROPOSED DATES
	Strike Expert Testimony, or Daubert Motions)	
Deadline to File Opening Briefs for Daubert Motions and Motions to Strike		Thursday, October 15, 2020
Deadline to File Responsive Briefs for Daubert Motions and Motions to Strike		Thursday, October 29, 2020
Deadline to File Reply Briefs for Daubert Motions and Motions to Strike		Thursday, November 5, 2020
Hearings on Daubert Motions and Motions to Strike		Thursday, November 19, 2020 (or availability of the Court)
Deadline to Serve Pretrial Disclosures (Witness List, Deposition Designations, and Exhibit List)	Friday, May 31, 2019	Wednesday, December 9, 2020
Deadline to Serve Objections to Pretrial Disclosures	Friday, June 14, 2019	Wednesday, December 23, 2020
Lead counsel meet & confer re settlement, preparation of the Joint Pretrial Statement and Order, preparation and exchange of pretrial materials, and clarification and narrowing of contested issues (Standing Order Re Final Pretrial Conference—Judge Freeman)	Thursday, June 20, 2019	Thursday, January 7, 2021
Deadline to Serve Motions *in Limine*	Tuesday, June 25, 2019	Thursday, January 14, 2021
Deadline to file "Pretrial Filings" (Joint Pretrial Statement, Trial Briefs, Compiled Briefing on Motions *in Limine*, Proposed Jury Instructions, Proposed Verdict Form, Proposed *Voir Dire* Questions, Witness List and Exhibit List) (Standing Order Re Final Pretrial Conference—Judge Freeman)	Thursday, June 27, 2019	Thursday, January 21, 2021
Deadline to Serve Responses to Motions *in Limine*	Wednesday, July 3, 2019	Thursday, January 28, 2021
Final Pretrial Conference (Pretrial Standing Order Re Final Pretrial Conference—Judge Freeman, ". . . approximately 2 weeks before trial")	Thursday, July 11, 2019 (subject to the convenience of the Court's calendar)	Thursday, February 4, 2021 (or availability of the Court)
Trial Date	Monday, July 29, 2019 (subject to the convenience of the Court's calendar)	Monday, March 1, 2021 (or availability of the Court)

ATTESTATION

I hereby attest under penalty of perjury that concurrence in the filing of this document has been obtained from counsel for Defendants.

Dated: December 14, 2017

BUNSOW DE MORY LLP

By: */s/ Henry C. Bunsow*
Henry C. Bunsow

Counsel for Plaintiff
VLSI TECHNOLOGY LLC

CASE MANAGEMENT ORDER

The above JOINT CASE MANAGEMENT STATEMENT & PROPOSED ORDER is approved as the Case Management Order for this case and all parties shall comply with its provisions. [In addition, the Court makes the further orders stated below:]

IT IS SO ORDERED.

Dated: _____

_____
The Hon. Beth Labson Freeman
UNITED STATES DISTRICT JUDGE